**Oscar Alejandro Manzano**

**EE 4513 VLSI**

**Report Lab 11**

**November 13, 2019**

For this lab, I used a code from lab8, but this time I used a different program to compare it’s time, area, and power. Synopsys Design Compiler which is the competition to cadence as I go through the program it seem pretty easy to used as seem below I was able to get all the information that I got in lab8.

Fall 2019

# EE 4513 – Introduction to VLSI Design

**Assignment # 11**

The objective of this assignment is to get familiar with the Synopsys Design Compiler tool.

1. Use the Verilog files you created for lab 8 for (i) 64 x 64 Array Multiplier

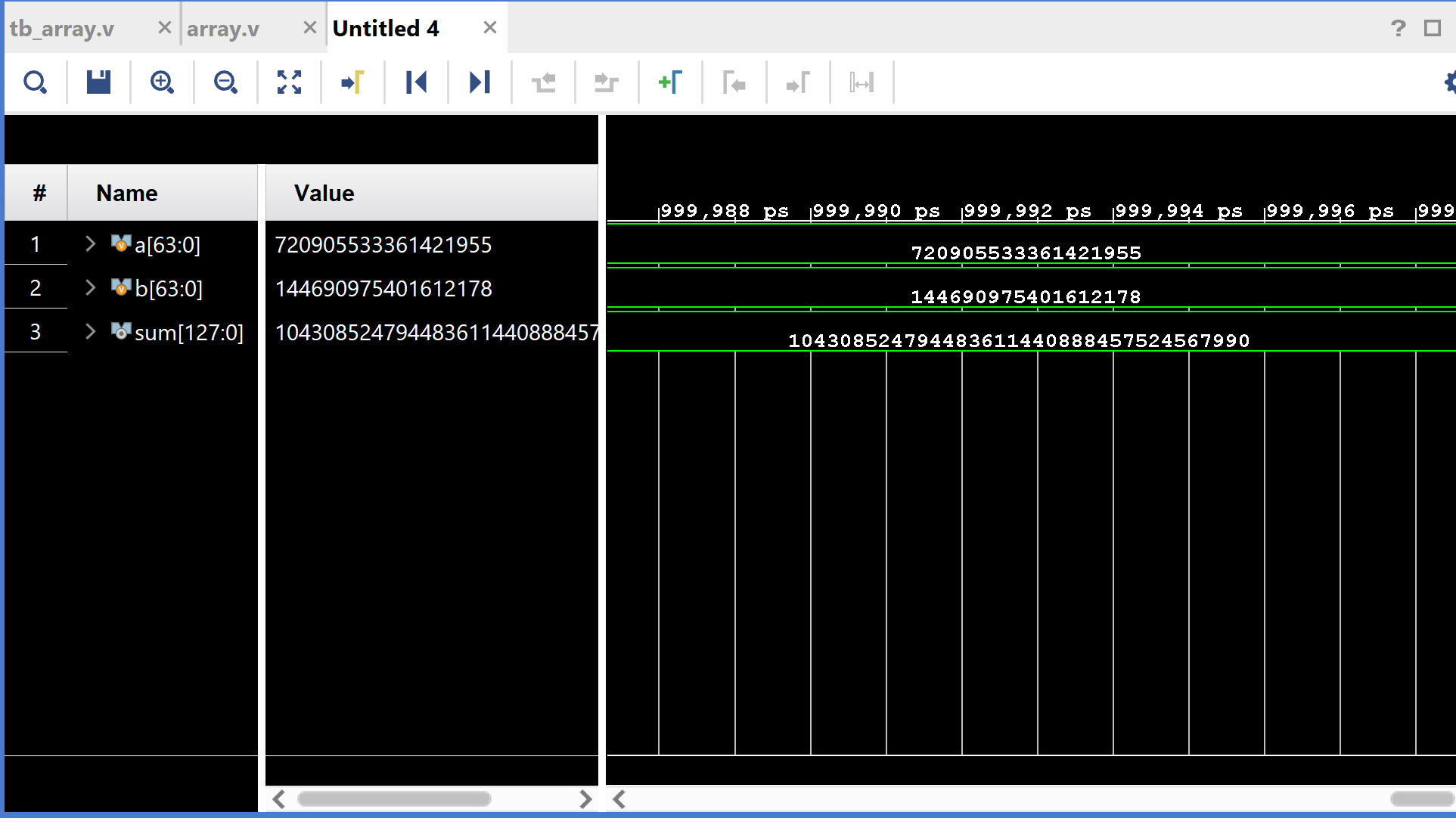
1. You have already completed the behavioral simulation (for example, using Vivado).

1. Then, use the Synopsys Design Compiler to generate gate level HDL netlists.

Verify your design for timing, area and power for both 45nm and 90nm Technology.

Turn in report, which includes the following: -

* 1. Simulation waveforms for your adder (Showing Time lags, any delays if u encounter)



* 1. Snapshots of Timing report, Area report and Power report for both 45nm and 90nm Technology.

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Information: Updating design information... (UID-85)

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Report : timing

-path full

-delay max

-max\_paths 1

Design : Array\_Mult

Version: L-2016.03-SP2

Date : Wed Nov 13 18:18:05 2019

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Operating Conditions: WORST Library: saed90nm\_max

Wire Load Model Mode: enclosed

Startpoint: b[63] (input port)

Endpoint: sum[126] (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

Array\_Mult 280000 saed90nm\_max

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 f

b[63] (in) 0.00 0.00 f

U4878/ZN (INVX0) 12069.43 12069.43 r

U8970/Q (AO221X1) 771.00 12840.43 r

U8971/QN (NOR2X0) 2.20 12842.63 f

U8972/Q (AO21X1) 2.36 12844.99 f

U9009/S (FADDX1) 2.62 12847.60 f

U17385/S (FADDX1) 2.56 12850.17 f

U8964/ZN (INVX0) 0.52 12850.69 r

U14864/S (FADDX1) 2.16 12852.85 f

intadd\_131/U3/S (FADDX1) 2.63 12855.48 f

U17345/CO (FADDX1) 2.69 12858.17 f

U15012/ZN (INVX0) 0.53 12858.71 r

intadd\_27/U3/S (FADDX1) 2.69 12861.40 f

U17528/S (FADDX1) 2.51 12863.91 r

intadd\_0/U64/CO (FADDX1) 2.84 12866.75 r

intadd\_0/U63/CO (FADDX1) 2.05 12868.80 r

intadd\_0/U62/CO (FADDX1) 2.05 12870.85 r

intadd\_0/U61/CO (FADDX1) 2.05 12872.90 r

intadd\_0/U60/CO (FADDX1) 2.05 12874.95 r

intadd\_0/U59/CO (FADDX1) 2.05 12877.00 r

intadd\_0/U58/CO (FADDX1) 2.05 12879.05 r

intadd\_0/U57/CO (FADDX1) 2.05 12881.10 r

intadd\_0/U56/CO (FADDX1) 2.05 12883.15 r

intadd\_0/U55/CO (FADDX1) 2.05 12885.20 r

intadd\_0/U54/CO (FADDX1) 2.05 12887.25 r

intadd\_0/U53/CO (FADDX1) 2.05 12889.30 r

intadd\_0/U52/CO (FADDX1) 2.05 12891.36 r

intadd\_0/U51/CO (FADDX1) 2.05 12893.41 r

intadd\_0/U50/CO (FADDX1) 2.05 12895.46 r

intadd\_0/U49/CO (FADDX1) 2.05 12897.51 r

intadd\_0/U48/CO (FADDX1) 2.05 12899.56 r

intadd\_0/U47/CO (FADDX1) 2.05 12901.61 r

intadd\_0/U46/CO (FADDX1) 2.05 12903.66 r

intadd\_0/U45/CO (FADDX1) 2.05 12905.71 r

intadd\_0/U44/CO (FADDX1) 2.05 12907.76 r

intadd\_0/U43/CO (FADDX1) 2.05 12909.81 r

intadd\_0/U42/CO (FADDX1) 2.05 12911.86 r

intadd\_0/U41/CO (FADDX1) 2.05 12913.91 r

intadd\_0/U40/CO (FADDX1) 2.05 12915.96 r

intadd\_0/U39/CO (FADDX1) 2.05 12918.02 r

intadd\_0/U38/CO (FADDX1) 2.05 12920.07 r

intadd\_0/U37/CO (FADDX1) 2.05 12922.12 r

intadd\_0/U36/CO (FADDX1) 2.05 12924.17 r

intadd\_0/U35/CO (FADDX1) 2.05 12926.22 r

intadd\_0/U34/CO (FADDX1) 2.05 12928.27 r

intadd\_0/U33/CO (FADDX1) 2.05 12930.32 r

intadd\_0/U32/CO (FADDX1) 2.05 12932.37 r

intadd\_0/U31/CO (FADDX1) 2.05 12934.42 r

intadd\_0/U30/CO (FADDX1) 2.05 12936.47 r

intadd\_0/U29/CO (FADDX1) 2.05 12938.52 r

intadd\_0/U28/CO (FADDX1) 2.05 12940.57 r

intadd\_0/U27/CO (FADDX1) 2.05 12942.62 r

intadd\_0/U26/CO (FADDX1) 2.05 12944.68 r

intadd\_0/U25/CO (FADDX1) 2.05 12946.73 r

intadd\_0/U24/CO (FADDX1) 2.05 12948.78 r

intadd\_0/U23/CO (FADDX1) 2.05 12950.83 r

intadd\_0/U22/CO (FADDX1) 2.05 12952.88 r

intadd\_0/U21/CO (FADDX1) 2.05 12954.93 r

intadd\_0/U20/CO (FADDX1) 2.05 12956.98 r

intadd\_0/U19/CO (FADDX1) 2.05 12959.03 r

intadd\_0/U18/CO (FADDX1) 2.05 12961.08 r

intadd\_0/U17/CO (FADDX1) 2.05 12963.13 r

intadd\_0/U16/CO (FADDX1) 2.05 12965.18 r

intadd\_0/U15/CO (FADDX1) 2.05 12967.23 r

intadd\_0/U14/CO (FADDX1) 2.05 12969.29 r

intadd\_0/U13/CO (FADDX1) 2.05 12971.34 r

intadd\_0/U12/CO (FADDX1) 2.05 12973.39 r

intadd\_0/U11/CO (FADDX1) 2.05 12975.44 r

intadd\_0/U10/CO (FADDX1) 2.05 12977.49 r

intadd\_0/U9/CO (FADDX1) 2.05 12979.54 r

intadd\_0/U8/CO (FADDX1) 2.05 12981.59 r

intadd\_0/U7/CO (FADDX1) 2.05 12983.64 r

intadd\_0/U6/CO (FADDX1) 2.05 12985.69 r

intadd\_0/U5/CO (FADDX1) 2.05 12987.74 r

intadd\_0/U4/CO (FADDX1) 2.05 12989.79 r

intadd\_0/U3/CO (FADDX1) 2.05 12991.84 r

U17556/S (FADDX1) 2.10 12993.95 f

U17096/ZN (INVX0) 0.45 12994.39 r

sum[126] (out) 0.00 12994.39 r

data arrival time 12994.39

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(Path is unconstrained)

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Report : power

-analysis\_effort low

Design : Array\_Mult

Version: L-2016.03-SP2

Date : Wed Nov 13 18:18:05 2019

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Library(s) Used:

saed90nm\_max (File: /var/lib/synopsys/synopsys\_90nm/synopsys/models/saed90nm\_max.db)

Operating Conditions: WORST Library: saed90nm\_max

Wire Load Model Mode: enclosed

Design Wire Load Model Library

------------------------------------------------

Array\_Mult 280000 saed90nm\_max

Global Operating Voltage = 0.7

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000ff

Time Units = 1ns

Dynamic Power Units = 1uW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = 774.7399 uW (65%)

Net Switching Power = 416.4587 uW (35%)

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Total Dynamic Power = 1.1912 mW (100%)

Cell Leakage Power = 494.1554 uW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational 774.7429 416.4583 4.9416e+08 1.6854e+03 ( 100.00%)

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Total 774.7429 uW 416.4583 uW 4.9416e+08 pW 1.6854e+03 uW

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Report : area

Design : Array\_Mult

Version: L-2016.03-SP2

Date : Wed Nov 13 18:18:05 2019

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Library(s) Used:

saed90nm\_max (File: /var/lib/synopsys/synopsys\_90nm/synopsys/models/saed90nm\_max.db)

Number of ports: 256

Number of nets: 17476

Number of cells: 14684

Number of combinational cells: 14684

Number of sequential cells: 0

Number of macros/black boxes: 0

Number of buf/inv: 1960

Number of references: 26

Combinational area: 161458.790422

Buf/Inv area: 10838.016281

Noncombinational area: 0.000000

Macro/Black Box area: 0.000000

Net Interconnect area: 22970.542038

Total cell area: 161458.790422

Total area: 184429.332460

1

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45nm

Information: Updating design information... (UID-85)

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Report : timing

-path full

-delay max

-max\_paths 1

Design : Array\_Mult

Version: L-2016.03-SP2

Date : Wed Nov 13 18:17:59 2019

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Operating Conditions: slow Library: NangateOpenCellLibrary

Wire Load Model Mode: top

Startpoint: b[2] (input port)

Endpoint: sum[126] (output port)

Path Group: (none)

Path Type: max

Des/Clust/Port Wire Load Model Library

------------------------------------------------

Array\_Mult 5K\_hvratio\_1\_1 NangateOpenCellLibrary

Point Incr Path

-----------------------------------------------------------

input external delay 0.00 0.00 f

b[2] (in) 0.00 0.00 f

U4319/ZN (INV\_X1) 0.61 0.61 r

U17121/ZN (NOR2\_X1) 0.26 0.87 f

U17255/ZN (NAND2\_X1) 0.29 1.16 r

U17256/ZN (OAI21\_X1) 0.15 1.31 f

U17257/ZN (INV\_X1) 0.17 1.48 r

U17258/ZN (OAI21\_X1) 0.11 1.59 f

intadd\_81/U8/CO (FA\_X1) 0.41 2.00 f

intadd\_81/U7/S (FA\_X1) 0.54 2.54 r

U13351/ZN (INV\_X1) 0.09 2.62 f

intadd\_288/U2/CO (FA\_X1) 0.40 3.03 f

U13346/ZN (INV\_X1) 0.20 3.23 r

intadd\_81/U6/CO (FA\_X1) 0.32 3.55 r

intadd\_81/U5/CO (FA\_X1) 0.30 3.85 r

intadd\_81/U4/CO (FA\_X1) 0.30 4.14 r

intadd\_81/U3/CO (FA\_X1) 0.30 4.44 r

intadd\_81/U2/CO (FA\_X1) 0.23 4.67 r

U13296/ZN (INV\_X1) 0.08 4.76 f

intadd\_1/U23/CO (FA\_X1) 0.42 5.17 f

intadd\_1/U22/CO (FA\_X1) 0.40 5.58 f

intadd\_1/U21/CO (FA\_X1) 0.40 5.98 f

intadd\_1/U20/CO (FA\_X1) 0.40 6.38 f

intadd\_1/U19/CO (FA\_X1) 0.40 6.78 f

intadd\_1/U18/CO (FA\_X1) 0.40 7.19 f

intadd\_1/U17/CO (FA\_X1) 0.40 7.59 f

intadd\_1/U16/CO (FA\_X1) 0.40 7.99 f

intadd\_1/U15/CO (FA\_X1) 0.40 8.39 f

intadd\_1/U14/CO (FA\_X1) 0.40 8.80 f

intadd\_1/U13/CO (FA\_X1) 0.40 9.20 f

intadd\_1/U12/CO (FA\_X1) 0.40 9.60 f

intadd\_1/U11/CO (FA\_X1) 0.40 10.01 f

intadd\_1/U10/CO (FA\_X1) 0.40 10.41 f

intadd\_1/U9/CO (FA\_X1) 0.40 10.81 f

intadd\_1/U8/CO (FA\_X1) 0.40 11.21 f

intadd\_1/U7/CO (FA\_X1) 0.40 11.62 f

intadd\_1/U6/CO (FA\_X1) 0.40 12.02 f

intadd\_1/U5/CO (FA\_X1) 0.40 12.42 f

intadd\_1/U4/CO (FA\_X1) 0.40 12.82 f

intadd\_1/U3/CO (FA\_X1) 0.40 13.23 f

intadd\_1/U2/CO (FA\_X1) 0.36 13.58 f

U12379/ZN (INV\_X1) 0.20 13.79 r

intadd\_5/U4/CO (FA\_X1) 0.32 14.10 r

intadd\_5/U3/CO (FA\_X1) 0.30 14.40 r

intadd\_5/U2/CO (FA\_X1) 0.23 14.63 r

U12182/ZN (INV\_X1) 0.09 14.72 f

intadd\_0/U92/CO (FA\_X1) 0.45 15.17 f

intadd\_0/U91/CO (FA\_X1) 0.40 15.57 f

intadd\_0/U90/CO (FA\_X1) 0.40 15.97 f

intadd\_0/U89/CO (FA\_X1) 0.40 16.38 f

intadd\_0/U88/CO (FA\_X1) 0.40 16.78 f

intadd\_0/U87/CO (FA\_X1) 0.40 17.18 f

intadd\_0/U86/CO (FA\_X1) 0.40 17.58 f

intadd\_0/U85/CO (FA\_X1) 0.40 17.99 f

intadd\_0/U84/CO (FA\_X1) 0.40 18.39 f

intadd\_0/U83/CO (FA\_X1) 0.40 18.79 f

intadd\_0/U82/CO (FA\_X1) 0.40 19.19 f

intadd\_0/U81/CO (FA\_X1) 0.40 19.60 f

intadd\_0/U80/CO (FA\_X1) 0.40 20.00 f

intadd\_0/U79/CO (FA\_X1) 0.40 20.40 f

intadd\_0/U78/CO (FA\_X1) 0.40 20.80 f

intadd\_0/U77/CO (FA\_X1) 0.40 21.21 f

intadd\_0/U76/CO (FA\_X1) 0.40 21.61 f

intadd\_0/U75/CO (FA\_X1) 0.40 22.01 f

intadd\_0/U74/CO (FA\_X1) 0.40 22.41 f

intadd\_0/U73/CO (FA\_X1) 0.40 22.82 f

intadd\_0/U72/CO (FA\_X1) 0.40 23.22 f

intadd\_0/U71/CO (FA\_X1) 0.40 23.62 f

intadd\_0/U70/CO (FA\_X1) 0.40 24.02 f

intadd\_0/U69/CO (FA\_X1) 0.40 24.43 f

intadd\_0/U68/CO (FA\_X1) 0.40 24.83 f

intadd\_0/U67/CO (FA\_X1) 0.40 25.23 f

intadd\_0/U66/CO (FA\_X1) 0.40 25.63 f

intadd\_0/U65/CO (FA\_X1) 0.40 26.04 f

intadd\_0/U64/CO (FA\_X1) 0.40 26.44 f

intadd\_0/U63/CO (FA\_X1) 0.40 26.84 f

intadd\_0/U62/CO (FA\_X1) 0.40 27.24 f

intadd\_0/U61/CO (FA\_X1) 0.40 27.65 f

intadd\_0/U60/CO (FA\_X1) 0.40 28.05 f

intadd\_0/U59/CO (FA\_X1) 0.40 28.45 f

intadd\_0/U58/CO (FA\_X1) 0.40 28.85 f

intadd\_0/U57/CO (FA\_X1) 0.40 29.26 f

intadd\_0/U56/CO (FA\_X1) 0.40 29.66 f

intadd\_0/U55/CO (FA\_X1) 0.40 30.06 f

intadd\_0/U54/CO (FA\_X1) 0.40 30.46 f

intadd\_0/U53/CO (FA\_X1) 0.40 30.87 f

intadd\_0/U52/CO (FA\_X1) 0.40 31.27 f

intadd\_0/U51/CO (FA\_X1) 0.40 31.67 f

intadd\_0/U50/CO (FA\_X1) 0.40 32.07 f

intadd\_0/U49/CO (FA\_X1) 0.40 32.48 f

intadd\_0/U48/CO (FA\_X1) 0.40 32.88 f

intadd\_0/U47/CO (FA\_X1) 0.40 33.28 f

intadd\_0/U46/CO (FA\_X1) 0.40 33.68 f

intadd\_0/U45/CO (FA\_X1) 0.40 34.09 f

intadd\_0/U44/CO (FA\_X1) 0.40 34.49 f

intadd\_0/U43/CO (FA\_X1) 0.40 34.89 f

intadd\_0/U42/CO (FA\_X1) 0.40 35.29 f

intadd\_0/U41/CO (FA\_X1) 0.40 35.70 f

intadd\_0/U40/CO (FA\_X1) 0.40 36.10 f

intadd\_0/U39/CO (FA\_X1) 0.40 36.50 f

intadd\_0/U38/CO (FA\_X1) 0.40 36.90 f

intadd\_0/U37/CO (FA\_X1) 0.40 37.31 f

intadd\_0/U36/CO (FA\_X1) 0.40 37.71 f

intadd\_0/U35/CO (FA\_X1) 0.40 38.11 f

intadd\_0/U34/CO (FA\_X1) 0.40 38.51 f

intadd\_0/U33/CO (FA\_X1) 0.40 38.92 f

intadd\_0/U32/CO (FA\_X1) 0.40 39.32 f

intadd\_0/U31/CO (FA\_X1) 0.40 39.72 f

intadd\_0/U30/CO (FA\_X1) 0.40 40.12 f

intadd\_0/U29/CO (FA\_X1) 0.40 40.53 f

intadd\_0/U28/CO (FA\_X1) 0.40 40.93 f

intadd\_0/U27/CO (FA\_X1) 0.40 41.33 f

intadd\_0/U26/CO (FA\_X1) 0.40 41.73 f

intadd\_0/U25/CO (FA\_X1) 0.40 42.14 f

intadd\_0/U24/CO (FA\_X1) 0.40 42.54 f

intadd\_0/U23/CO (FA\_X1) 0.40 42.94 f

intadd\_0/U22/CO (FA\_X1) 0.40 43.34 f

intadd\_0/U21/CO (FA\_X1) 0.40 43.75 f

intadd\_0/U20/CO (FA\_X1) 0.40 44.15 f

intadd\_0/U19/CO (FA\_X1) 0.40 44.55 f

intadd\_0/U18/CO (FA\_X1) 0.40 44.96 f

intadd\_0/U17/CO (FA\_X1) 0.40 45.36 f

intadd\_0/U16/CO (FA\_X1) 0.40 45.76 f

intadd\_0/U15/CO (FA\_X1) 0.40 46.16 f

intadd\_0/U14/CO (FA\_X1) 0.40 46.57 f

intadd\_0/U13/CO (FA\_X1) 0.40 46.97 f

intadd\_0/U12/CO (FA\_X1) 0.40 47.37 f

intadd\_0/U11/CO (FA\_X1) 0.40 47.77 f

intadd\_0/U10/CO (FA\_X1) 0.40 48.18 f

intadd\_0/U9/CO (FA\_X1) 0.40 48.58 f

intadd\_0/U8/CO (FA\_X1) 0.40 48.98 f

intadd\_0/U7/CO (FA\_X1) 0.40 49.38 f

intadd\_0/U6/CO (FA\_X1) 0.40 49.79 f

intadd\_0/U5/CO (FA\_X1) 0.40 50.19 f

intadd\_0/U4/CO (FA\_X1) 0.40 50.59 f

intadd\_0/U3/CO (FA\_X1) 0.40 50.99 f

intadd\_0/U2/S (FA\_X1) 0.54 51.53 r

U4439/ZN (INV\_X1) 0.04 51.58 f

sum[126] (out) 0.00 51.58 f

data arrival time 51.58

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(Path is unconstrained)

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Report : power

-analysis\_effort low

Design : Array\_Mult

Version: L-2016.03-SP2

Date : Wed Nov 13 18:18:00 2019

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Library(s) Used:

NangateOpenCellLibrary (File: /home/proj/FSM/Nangate/NangateOpenCellLibrary\_slow\_conditional\_nldm.db)

Operating Conditions: slow Library: NangateOpenCellLibrary

Wire Load Model Mode: top

Design Wire Load Model Library

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Array\_Mult 5K\_hvratio\_1\_1 NangateOpenCellLibrary

Global Operating Voltage = 0.95

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000pf

Time Units = 1ns

Dynamic Power Units = 1mW (derived from V,C,T units)

Leakage Power Units = 1pW

Cell Internal Power = 381.4622 uW (57%)

Net Switching Power = 290.3569 uW (43%)

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Total Dynamic Power = 671.8191 uW (100%)

Cell Leakage Power = 101.2248 uW

Information: report\_power power group summary does not include estimated clock tree power. (PWR-789)

Internal Switching Leakage Total

Power Group Power Power Power Power ( % ) Attrs

--------------------------------------------------------------------------------------------------

io\_pad 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

memory 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

black\_box 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

clock\_network 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

register 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

sequential 0.0000 0.0000 0.0000 0.0000 ( 0.00%)

combinational 0.3815 0.2904 1.0122e+08 0.7730 ( 100.00%)

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Total 0.3815 mW 0.2904 mW 1.0122e+08 pW 0.7730 mW

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Report : area

Design : Array\_Mult

Version: L-2016.03-SP2

Date : Wed Nov 13 18:18:00 2019

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Library(s) Used:

NangateOpenCellLibrary (File: /home/proj/FSM/Nangate/NangateOpenCellLibrary\_slow\_conditional\_nldm.db)

Number of ports: 256

Number of nets: 17748

Number of cells: 14936

Number of combinational cells: 14936

Number of sequential cells: 0

Number of macros/black boxes: 0

Number of buf/inv: 2810

Number of references: 25

Combinational area: 22289.470061

Buf/Inv area: 1497.048015

Noncombinational area: 0.000000

Macro/Black Box area: 0.000000

Net Interconnect area: 7311.684767

Total cell area: 22289.470061

Total area: 29601.154828

* 1. A comparison of delay, area and power for 45nm and 90 nm technology nodes.

45nm

data arrival time 51.58

Total cell area: 22289.470061

Total 0.3815 mW 0.2904 mW 1.0122e+08 pW 0.7730 mW

90nm

Total cell area: 161458.790422

Total 774.7429 uW 416.4583 uW 4.9416e+08 pW 1.6854e+03 uW

data arrival time 12994.39

For this comparison the 90nm did way worse than the 45nm in all areas power, time, an area.

**Note**: -

1. Once you have logged in, make a new directory called **lab11**. For example, if your account is abc.123, then upon login you will be taken to a directory with the same name. This is **your** home directory (not to be confused with another directory with the name ‘home’). To view the path of this directory, use the ‘pwd’ command. Then make the ‘lab11’ directory by using the **mkdir** command (**mkdir** **lab11**). Then change over to the lab11 directory using **cd lab11.** All the files relatedto this assignment should be in this directory. You must use the same names as mentioned here.